AMENDMENTS TO THE DRAWINGS

In the drawings, reference character "300" was omitted from FIG. 3. Applicants submit herewith a replacement sheet, where the missing reference character "300" is included in FIG. 3.

Replacement Sheet: Figure 3

REMARKS

In the Office Action, the Examiner noted that claims 1-21 are pending in the application, of which claims 20 and 21 are withdrawn from consideration. The Examiner rejected Claims 1-19. By this response, Claims 20 and 21 remain withdrawn subject to possible rejoinder. Claims 1, 3, 6, 10, and 12-13 are amended, and Claim 2 is cancelled. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Restriction Requirement

The Applicant affirms the election of Claims 1-19 (referred to as Group I) with traverse. Claims 20 and 21 have been withdrawn without prejudice.

II. Objections

The Examiner objected to the drawings as omitting a reference sign mentioned in the description. In particular, the Examiner stated that the reference character "300" is omitted from FIG. 3. Applicants submit herewith a replacement sheet, where the missing reference character "300" is included in FIG. 3. Accordingly, Applicants respectfully request that the objection to the drawings be withdrawn.

III. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1-19 as being anticipated by Wang et al. (United States patent 6,594,809, issued July 15, 2003). More specifically, the Examiner stated that Wang teaches selecting a block of standard cells, associating a diode circuit with at least one input port of the cell block to form an augmented block, and implementing the augmented block. (Office Action, p. 4). The rejection is respectfully traversed.

Wang discloses diode insertion for correcting antenna rule violations during the design and formation of integrated circuits. (Wang, Abstract). In particular, Wang states that, in the past, antenna diode cells were laid out during the initial placement process in sufficient number to assure that all conductors were in proximity to an

antenna diode cell. In this manner, diode(s) can be connected to the conductor(s) if an antenna rule violation later became apparent after the design rule check had been performed. (Wang, col. 4, lines 19-25). Wang then discloses a technique where standard cells defining a circuit are placed and routed. Filler cells are subsequently laid out, where at least some of the filler cells include a diode circuit. A design rule check is performed to identify antenna rule violations based on the routing of conductors previously performed. The antenna rule violations are then corrected by connecting the appropriate diode circuits with their adjacent conductors. (Wang, col. 5, lines 16-30).

Wang, however, does not teach each and every element of Applicants' invention recited in amended Claim 1. Namely, Wang does not teach or suggest laying out components along with diode circuit(s) associated with input port(s) and then routing conductors for connecting the components and connecting each of the input port(s) with the associated diode circuit. That is, in Applicants' invention recited in Claim 1, a given diode circuit is connected to its respective input port during routing of the components in the standard cell block. Applicants' Claim 1 specifically recites the step of "routing conductors for connecting said components and connecting each said at least one input port to said associated diode circuit." This is in contrast to the technique described in Wang, where the diode circuits are connected after the standard cells are routed and a design rule check has been performed to identify antenna rule violations. Wang does not teach or suggest connecting the diode circuits with their adjacent conductors during routing of the standard cells defining the circuit.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Wang does not teach connecting the diode circuits with their adjacent conductors during routing of the standard cells defining the circuit, Wang does not teach each and every element of Applicants' Claim 1 as arranged therein. Accordingly, Wang does not anticipate Applicants' invention recited in Claim 1. Claim 12 includes features similar to those of Claim 1 emphasized above. For the same

reasons set forth above, Applicants contend that Wang does not anticipate the invention of Claim 12.

In Applicants' Claim 14, diode circuits are associated with primary input ports of an embedded logic circuit, which is then placed, routed, and integrated with existing logic circuitry to form an integrated circuit. Wang does not specifically teach or suggest associating diode circuits with primary input ports of an embedded logic circuit. Rather, Wang generally states that diode circuits are associated with conductors. Moreover, Wang does not specifically teach or suggest placing, routing, and integrating an embedded logic circuit having the diode circuits with existing logic circuitry. Wang is devoid of any discussion regarding embedding logic with existing logic circuitry. As discussed above, Wang does not teach or suggest connecting the diode circuits with their adjacent conductors during routing of the standard cells defining the circuit. For these reasons, Applicants contend that Wang does not anticipate the invention of Claim 14.

Finally, Claims 3-11, 13, and 15-19 depend, either directly or indirectly, from Claims 1, 12, and 14 and recite additional features therefor. Since Wang does not anticipate Applicants' invention as recited in Claims 1, 12, and 14, dependent Claims 3-11, 13, and 15-19 are also not anticipated and are allowable. Therefore, Applicants contend that Claims 1 and 3-19 are not anticipated by Wang and, as such, fully satisfy the requirements of 35 U.S.C. §102.

CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Kim Kanzaki at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on May 16, 2006.

Pat Tompkins
Name

Pat Tompkins
Signature